A New Inquisitive Technique for Lessening Leakage in Domino Logic Circuits

K.Suhanandini, S.LakshmiNarayanan, ReebaKorah

ABSTRACT: The hasty technology scaling in the advancement of portable device designs, always has a tradeoff between power and performance. With respect to the various power dissipations static leakage started sharing its space equally with dynamic power in a progressive manner. The need for trimming down of leakage power in the diminutive devices for the performance up gradation is rising day by day. The approach accorded here is the introduction ofleakage reduction techniques for reducing the leakage power in Domino Logic circuits. Comparative study of leakage power in the Conventional AND circuit, Footed and Footerless Domino circuits is done. All these circuits are implemented with the introduction of Leakage controlled transistors. Analysis is also done with and without Adiabatic Logic separately. The Simulation is done in the Tanner tool and the results are studied based on the leakage Power.

KEYWORDS: Adiabatic, Footed Domino Logic, Footerless Domino Logic, Leakage Controlled Transistors, Leakage power, Pull Down Network, Stacking.

1 Introduction

Moore's law [1] states that the "number of transistors placed reasonably on an integrated circuit will double about every two years". This has often been subject to the following criticism: though it boldly states the blessing of technology scaling, it fails to uncover its bane. A consequence of Moore's law is that the "power density of the integrated circuit increases exponentially with each and every technology scaling". Dissipation of power in a transistor could be differentiated as dynamic, short circuit and leakage power dissipations. Leakage power in the nanometer regime is becoming the main donor for the power dissipation. Leakage in the transistor is due to the reduction made in the threshold voltage, length of the channel and the gate oxide thickness. Leakage mechanism includes the following categories:

REVERSE BIASED JUNCTION LEAKAGE (I_{REV})is due to the reverse bias current in the parasitic diodes formed between the diffusion region of the transistor and substrate. It results from the drift and diffusion of minority carriers near the edge of depletion regions, and also from the electron hole pair generation in the depletion regions of reverse-biased junctions.

- *Author: K.Suhanandiniis currently pursuing masters degree program in VLSI DESIGN in AIHT under Anna University,India. E-mail: suhanandini@gmail.com*
- *Author: S.LakshmiNarayananis currently working as a Assistant Professor in ECE Dept at AIHT under Anna University,India. E-mail:narayananrevs@gmail.com*
- *Author: ReebaKorahis currently working as a Professor in ECE Dept at St.Joseph's College of Engineering under Anna University,India. E-mail:reeba26in@gmail.com*

GATE INDUCED DRAIN LEAKAGE (I_{GIDL}) is caused by high field effect in the drain junction of MOS transistors.

GATE OXIDE TUNNELING (I_G)flows from the gate through the oxide insulation to the substrate.This current results from the Fowler-Nordheim tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer[3]. As oxides get thinner, this current could exceed many other smaller leakages. In oxide layers less than 3-4 nm thick, there can also be direct tunneling through the silicon oxide layer[2].

SUB-THRESHOLD LEAKAGEflows from the source to drain even if the gate to source voltage is below the threshold voltage of the device. This happens due to several reasons such as weak inversion effect, the Drain-Induced Barrier Lowering and the direct punch-through of the electrons between drain and source.

Sub-threshold leakage and the Gate-oxide tunneling form the dominating type of leakages, while others could be considered as negligible comparatively.

High-speed performance chips could be achieved by employing Domino Logic circuits. Generally these forms of circuits are classified as Footerless and Footed Domino's[4].A new approach for reduction of leakage in these types of Domino logic circuits is accorded in this work.

The remaining section of this paper is structured as follows: In Section 3 proposed domino logic circuit for reduction in leakage is described. Simulation results are presented in Section 4. Finally the conclusions are described in Section 5.

2 Leakage Analysis

This section includes the three subsections namely

2.1Leakage in the Conventional AND circuit, 2.2 Standard footed and footer less domino logic circuits.

2.1Leakage in the conventional AND circuit Representation of the conventional AND circuit isshown in the Fig 1. Simulation of this AND circuit is done in Tanner Tool and the output of this is represented in Fig 2. The Leakage power dissipation is measured for the circuit and the result is represented in Fig 6.

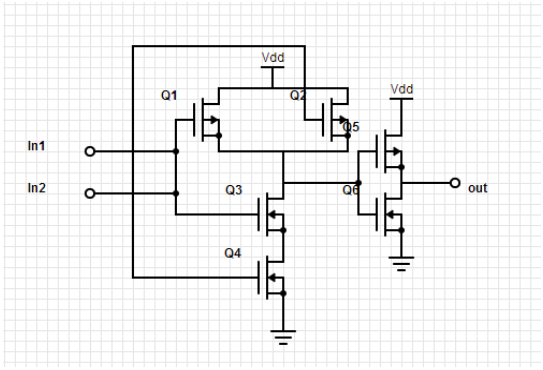

Fig 1. Conventional AND circuit

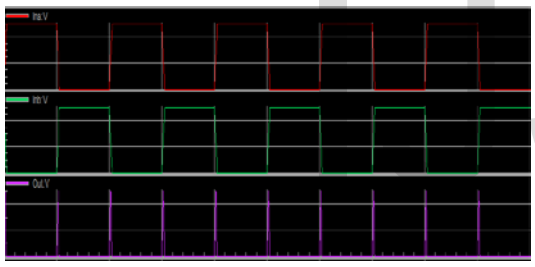

Fig 2. Output of Conventional AND

2.2 Standard Footed and Footless Domino Logic Circuits

High-speed performance chips could be achieved by employing Domino Logic circuits. Generally these forms of circuits are classified as Footerless and Footed Domino's[4]. Footed domino circuits are said to have better timing characteristics because of the isolation of the pull-down network (PDN) from ground by the evaluation transistor which prevents the change of state of the dynamic node during the precharge phase. In the other case, if the evaluation transistor or the Footer transistor is omitted, it leads to the reduction of the Power consumption and the evaluation delay. Both are used in performance high processors but in multi-stage domino circuits, all the stages are considered as footerless except for the first stage[5].

The basic structures of the Footed and Footerless domino logic AND circuits are represented in the Fig3&4.

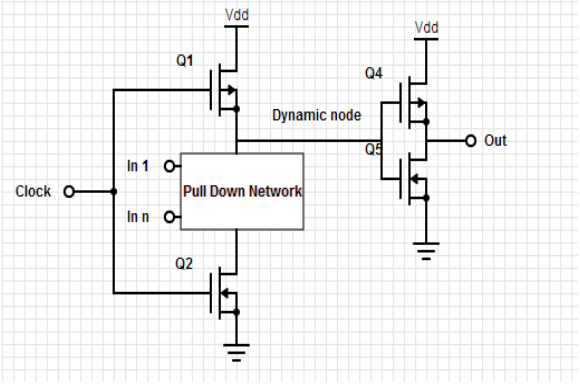

Fig 3. Footed DOMINO circuit

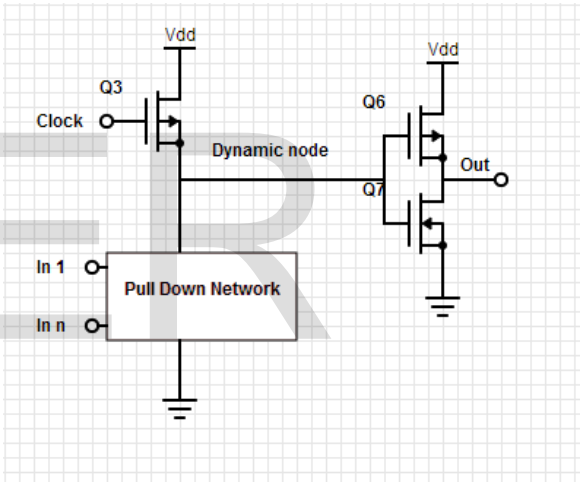

Fig4. Footer Less DOMINO Logic circuit

3 Proposed Domino Logic circuits

This section includes the proposed technique of implementing the leakage controlled transistors and the Adiabatic logic.

The proposed technique implemented in the domino logic circuit effectively reduces the leakage. Reduction of leakage power by introducing the Leakage Controlled transistors in the path formed from supply voltage to the ground is the notion behind this approach. Leakage controlled transistors consist of a p-type and n-type transistors with each of its gate connected to the source of the other. For every combination of input, either of the leakage controlled transistors will operate near its cut off region there by increasing the resistance along the supply voltage and ground path which in turn reduces the

leakage current. The proposed circuit for both the Footed and the Footer Less Domino Logic circuits isrepresented in Fig 3a &4a.

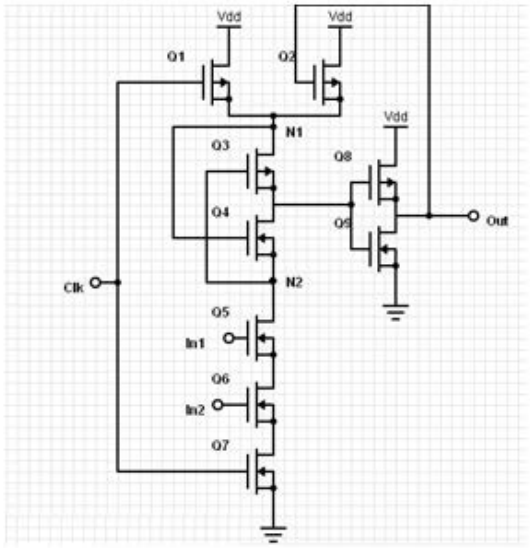

Fig 3a. Footed two input DOMINO AND circuit

Here, the PMOS transistor Q3 and the NMOS transistor Q4 are introduced between the clocked transistors. Each gate is connected to the source of the other transistor. The drain nodes of both the transistors are connected together and this is the input of the inverter. In this formation, transistor Q3 and Q4 switching depends upon the voltage potential at two nodes N1, N2. So any combination of input in the pull-down network will make one of the LCT's to operate its cut-off region and this increases the resistance between the V_{dd} and ground leading to the leakage power reduction.

The working of the proposed circuit of Footerless AND is as follows: When the clock is low or in the non-ideal mode the dynamic node is charged high through the transistor Q1 and Q3. The charging of dynamic node is almost independent of the previous clock input state. Before the clock is set to low if the inputs are low, then there will be a low potential at the node N2 and Q3 transistor offers a less resistance path for charging the dynamic node. And if the inputs are high before the clock is low then the voltage at node N2 will not be sufficient in turning OFF Q3 completely. The resistance of Q3 will be lower than in the OFF resistance letting the dynamic node charging high. The charging of the dynamic node is said to be the precharging phase.

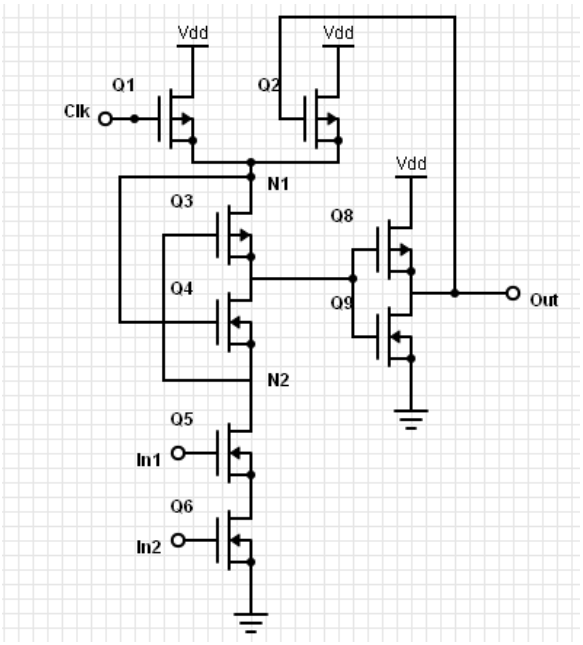

Fig 4a.Footer Less two input DOMINO AND circuit

In the evaluation phase, where the clock turns high say, the ideal mode, based on the inputs the dynamic node will get charged or discharged. When all the inputs are low, the transistors in the pull down network will not get switched ON and so the dynamic node will not be discharged by the evaluation network and so the output of the inverter will be low. This will turn ON the transistor Q2, thereby the voltage at the node N1 will turn ON the transistor Q9, high resistance path between VDD and ground reducing sub-threshold and gate leakage current is produced by the voltage induced at the node N2 which will not cut off the transistor Q3 and will operate near the cut off region. Discharging of the dynamic node happens when all the inputs are high and now the output of the inverter will be high. Q2 will now turn OFF, and with the voltage at node N1 the transistor Q4 will operate near its cut off region once again producing a high resistance path.The potential at node N2 will turn ON the transistor Q3. This shows that because of the introduction of the LCTs a resistivity will be increased along the path from voltage supply and the ground which will tend to the reduction of the leakage power. Propagation delay also gets reduced because of this [5].

The same kind of operation takes place in the case of Footed Domino logic circuits also but with the absence of the footer transistor (the clocked evaluation NMOS transistor). The Footed Domino Logic circuit with LCT's is represented in Fig 3a.

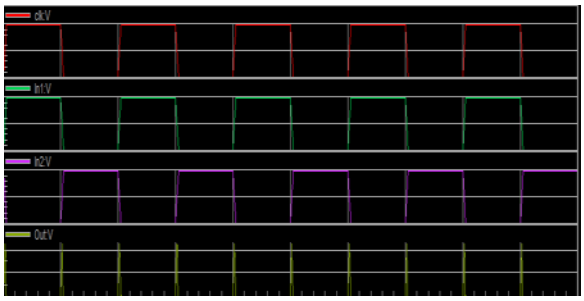

Fig 5. Output of two input DOMINO AND circuits

In the above three circuits (Conventional AND, Footed Domino AND and Footer less Domino AND) in addition to the insertion of LCT's the Adiabatic logic is also implemented.A new and simple technique with a different approach for reducing the power dissipation in digital logic circuits is emerging now-a-days. This approach makes a change in the power supply which is being a DC supply in most of the cases. When periodic signals are used instead of DC, the energy getting dissipated as heat can be recovered by recycling of signal energies in the circuit capacitances could be achieved and this could be restored for reuse. The ideal energy dissipation of a circuit when a capacitance C is charged from 0 to V_{dd} or discharged from V_{dd} to 0 through a circuit of resistance R,at time T is given by,

$$E = \left(\frac{RC}{T}\right)(V_{dd})^2 \qquad (1)$$

Where E represents the energy dissipation, R is the resistance, Tis the Temperature, C is the Capacitance and V_{dd} is the Supply Voltage. Here when "T >> RC", the power consumption is much smaller than the conventional CMOS circuit, for which an energy of "$\left(\frac{1}{2}\right)\left(C(V_{dd})^2\right)$" is required during a charge or discharge cycle [8]. In a transistor the charge on the gate is called the controlling charge and the charge flowing from the drain to source is called as the controlled charge. The energy dissipation in the transistors is because of the resistance offered by the channel to the controlled charge. This can be minimized when the charge transport in the channel is slowed [9]. When circuits are made to operate in the adiabatic region with subsequently low energy dissipation, the energy used for charging the capacitive signal nodes of the circuit might be recovered when discharging takes place and could be stored for reuse. In such kind of circuits the efficiency is limited only by the adiabaticity of the energy transfers. Most of the Conventional CMOS circuits are mostly non adiabatic capacitive signal nodes that get charged and discharged quickly. It is seen from the results that the circuits with adiabatic logic implementation has lesser power dissipation than the same circuits without Adiabatic implementation.

The conventional AND circuit, the footed Domino AND circuit and the Footer less Domino AND circuits are implemented with the Leakage Controlled Transistors, the Adiabatic Logic and analysis was done based on the leakage power.

4 Simulation Results

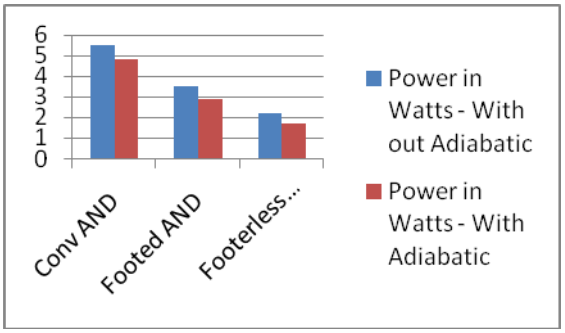

Fig 6. Simulation Results

Simulation results show that Conventional 2 input AND circuits have more leakage than Domino Logic circuits. Among the different types of Domino circuits, Footed circuits have more leakage than the FooterLess circuits. Also when Adiabatic logic is implemented, these circuits have lesser leakage with Adiabatic logic implementation than its counterparts.

5 Conclusion

In the scaling of nm technologies the leakage currents must be suppressed for reducing power dissipation. With this intension, the above mentioned circuit techniques are proposed for the reduction of currents in the domino logic circuits. The proposed domino circuit technique holds the implementation of LCT's which is quite similarto the stacking effect. This is introduced in the path formed between the VDD and the ground, say precharge and the evaluation network. The combination of both the LCT implementation and the adiabatic logic show a good reduction of leakage current in the Domino logic circuits. Comparison of the Conventional AND Circuit, Footed Domino AND circuit with LCT's and the Footer less AND circuit with LCT's is done. All these three circuits were implemented with Adiabatic logic also. Results show that the Footer less circuit with LCT had lesser leakage than the Footed one with LCT, which had lesser leakage than the Conventional AND. Also circuits with Adiabatic logic had lesser leakage than the circuits without adiabatic logic. The

total Leakage of the circuit can be calculated by the summation of the leakage measured for the individual transistors multiplied by its power supply.

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